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High Speed Low-Power Viterbi Decoder Using Trellis Code Modulation

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Abstract - High speed low power viterbi decoders for trellis code modulation is well known for the delay consumption in underwater communication. In transmission system wireless communication is the transfer of information between two or more points that are not connected by an electrical conductor. WiMAX is the wireless communication standard designed to provide 30 to 40 Mega bits per second data rates. WiMAX as a standards based technology enabling the delivery of last mile wireless broadband access as an alternative to cable and DSL. WiMAX can provide at home or mobile internet access across whole cities or countries. The address generation of WiMAX is carried out by interleaver and deinterleaver. Interleaving is used to overcome correlated channel noise such as burst error or fading. The interleaver/deinterleaver rearranges input data such that consecutive data are spaced apart. The interleaved memory is to improve the speed of access to memory. The viterbi technique reduces the bit error rate and delay using wimax.

Keywords-WiMAX, Interleaver, Deinterleaver, Viterbi encoding/decoding

I. INTRODUCTION

Broadband wireless access is continuously becoming a more challenging competitor to the conventional wired last mile access technologies. WiMAX stands for Worldwide Interoperability for Microwave Access, it is used as an alternative to cable and DSL.WLAN and WiMAX are emerging standards for wireless broadband communication system. In WiMAX transreceiver the channel interleaver is present which is used to minimize the effect of burst error. The interleaver rearranges the input data such that consecutive data are spaced apart. The deinterleaver in receiver side arranges the interleaved data into original sequence. The direct implementation of interleaver/deinterleaver functions in WiMAX is not hardware efficient due to the presence of complex function. In WiMAX application the address generation for deinterleaver using the modulation technique such as QPSK,16QAM and 64QAM. The 2-D transformation of WiMAX channel interleaver/deinterleaver functions reduces the overall hardware complexity to compute the deinterleaver address and also it eliminate the requirement of floor function. Compare to configurable logic block based multiplier the use of FPGA based embedded multiplier provides better performance. It reduces interconnection delay, efficient resource utilization and lower power consumption.

II. RELATED WORK

A few work related to the hardware implementation of interleaver/deinterleaver function in WiMAX system is available in the literature. The work shows the grouping of incoming data streams in to block to reduce the frequency of memory access in a deinterleaver using conventional look up table based address generator in WiMAX system. The work also shows that, it is finite state machine based technique is used to generate the address for interleaver/deinterleaver in WiMAX system. The modulation technique is used to eliminate the requirement of floor function while generating the write address. The 2D translation is made to claim efficient hardware architecture but not clearly explain the design, particularly for 64 quadrature amplitude modulation (QAM). Conventional LUT based technique is found to be unattractive from many aspects such as slowness in operation, consumption of large logic resources leading to inefficiency in resource utilization.

III.DESCRIPTION

The overview of WiMAX transreceiver is shown in figure 1. The input is given to the source and the output of the source is randomized before being encoded by two Forward Error Correction (FEC) techniques such as Reed Solomon 1398 (RS) and Convolutional Coding (CC). The channel interleaver allows the encoded bit stream to reduce the effect of burst error. The channel interleaver is not required when Convolutional turbo code is used for Forward Error Correction. The resulting data symbols are used to mapping and construct the orthogonal frequency division multiplexing is performed by two blocks namely mapper and inverse fast fourier transform. In receiver the blocks are arranged in the reverse order to restore the original data sequence at the output.

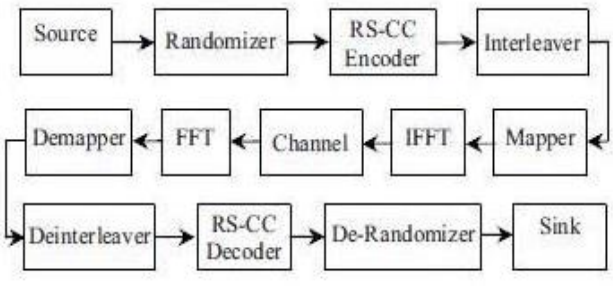

Fig 1: Overview of WiMAX Transreceiver

Reed Solomon code is a linear cyclic systematic non binary block code. A generator polynomial is used to generate the redundant symbols and it is appended to the message symbols, in the encoder. The same generator polynomial is used to calculate the error location and magnitude in decoder. Then the correction is applied on the received code. Instead of reed solomon code the viterbi algorithm is used in WiMAX transreceiver. The viterbi algorithm is the optimum algorithm that reduces the probability of error.

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IV WiMAX CHANNEL INTERLEAVER

The interleaver memory block has two memory modules are M1, M2 and also has three mux and an inverter. In block interleaving when one memory block is being written and other is read and vice versa.

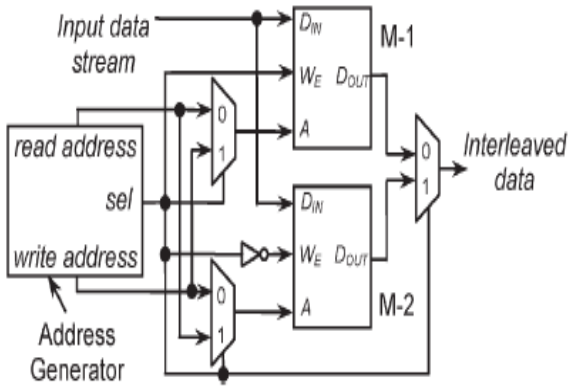

Fig 2: Interleaver/deinterleaver structure

The MUX connected to the address input and sel line are used to perform either read or write operation in each memory modules. When sel line = 1, the write enable signal in M1 is active and it generate write address, simultaneously M2 generate read address. After the read/write operation, it is stored in derived location and then the status of the sel signal is changed to exchange the read/write operation. The data stream obtained from the RS-CC encoder is permuted by using the two step processes described by (1) and (2). Thus

$$m_k = (N_{cbps}/d).(k\%d) + [k/d] \quad (1)$$

$$j_k = s.[m_k/s] + (m_k + N_{cbps} - [d.m_k/N_{cbps}]) \quad (2)$$

TABLE I

Permitted Interleaver/Deinterleaver Depth for All Code Rates and Modulation Type

Modulation Scheme	QPSK (s=1)		16 QAM (s=2)		64 QAM (s=3)		
Code Rate	1/2	3/4	1/2	¾	1/2	2/3	¾
Interleaver Depth, N_{cbps} in bits	96	144	192	288	288	384	432
	192	288	384	576	576	-	-
	288	432	576	-	-	-	-
	384	576	-	-	-	-	-
	480	-	-	-	-	-	-
	576	-	-	-	-	-	-

First Four Rows And Five Columns of Deinterleaver Sample Addresses For Three Code Rates and Modulation Schemes

TABLE II

N_{cbps}, code rate and modulation type	Deinterleaver address				
N_{cbps}=96-bits,1/2 code rate, QPSK	0	16	32	48	64
	1	17	33	49	65
	2	18	34	50	66
	3	19	35	51	67
N_{cbps}=192-bits,1/2 code rate,16QAM	0	16	32	48	64
	17	1	49	33	81
	2	18	34	50	66
	19	3	51	35	83
N_{cbps}=576-bits,3/4 code rate,64QAM	0	16	32	48	64
	17	33	1	65	81
	34	2	18	82	50
	3	19	35	51	67

V WiMAX CHANNEL DEINTERLEAVER

The deinterleaver performs the inverse operation, is also permuted by two step process. Let mj and kj define the first and level of permutation for the deinterleaver, where j is the received bit index within a block of Ncbps bits.

$$mj = s.[j/s] + (j + [d.j / Ncbps]) \%s \quad (3)$$

It ensures the adjacent coded bits are mapped on to nonadjacent carriers.

$$kj = d.mj - (Ncbps - 1) . [d.mj / Ncbps] \quad (4)$$

Eqns (3) and (4) perform inverse operation of (2) and (1) respectively.

$$k_{n,\mathrm{QPSK}} = \{ d * i + j \quad \text{for } \forall j \text{ and } \forall i \quad (5)$$

$$k_{n,\text{16-QAM}} = \begin{cases} d*i+j & \text{for } j\%2 = 0 \text{ and for } \forall i \\ d*(i+1)+j & \text{for } j\%2 = 1 \text{ and} \\ & \text{for } i\%2 = 0 \\ d*(i-1)+j & \text{for } j\%2 = 1 \text{ and} \\ & \text{for } i\%2 = 1 \end{cases} \quad (6)$$

$$k_{n,\text{64-QAM}} = \begin{cases} d*i+j & \text{for } j\%3 = 0 \text{ and for } \forall i \\ d*(i-2)+j & \text{for } j\%3 = 1 \text{ and} \\ & \text{for } i\%3 = 2 \\ d*(i+1)+j & \text{for } j\%3 = 1 \text{ and} \\ & \text{for } i\%3 \neq 2 \\ d*(i+2)+j & \text{for } j\%3 = 2 \text{ and} \\ & \text{for } i\%3 = 0 \\ d*(i-1)+j & \text{for } j\%3 = 2 \text{ and} \\ & \text{for } i\%3 \neq 0 \end{cases} \quad (7)$$

Where j = 0,1,…..,d-1 and i = 0,1,….,(Ncbps/d)-1 represent the row and column numbers and kn represents the deinterleaver addresses. The equation (5)-(7) represents the correlation between addresses of table III has been proven using algebraic analysis. The mathematical representation of (5)-(7) follows three algorithms for three modulation techniques. These algorithms eliminate the requirement of floor function while generating write addresses.

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TABLE III
Determination of Correlation Between Addresses

Row no.(j)	Column no. (i) →	0	1	2	3	4
0	N_{cbps} = 96-bits, ½ code rate, QPSK	d.0+0=0	d.1+0=16	d.2+0=32	d.3+0=48	d.4+0=64
1		d.0+1=1	d.1+1=17	d.2+1=33	d.3+1=49	d.4+1=65
2		d.0+2=2	d.1+2=18	d.2+2=34	d.3+2=50	d.4+2=66
3		d.0+3=3	d.1+3=19	d.2+3=35	d.3+3=51	d.4+3=67
0	N_{cbps} = 192-bits, ½ code rate, 16-QAM	d.0+0=0	d.1+0=16	d.2+0=32	d.3+0=48	d.4+0=64
1		d.1+1=17	d.0+1=1	d.3+1=49	d.2+1=33	d.5+1=81
2		d.0+2=2	d.1+2=18	d.2+2=34	d.3+2=50	d.4+2=66
3		d.1+3=19	d.0+3=3	d.3+3=51	d.2+3=35	d.5+3=83
0	N_{cbps} = 576-bits, ¾ code rate, 64-QAM	d.0+0=0	d.1+0=16	d.2+0=32	d.3+0=48	d.4+0=64
1		d.1+1=17	d.2+1=33	d.0+1=1	d.4+1=65	d.5+1=81
2		d.2+2=34	d.0+2=2	d.1+2=18	d.5+2=82	d.3+2=50
3		d.0+3=3	d.1+3=19	d.2+3=35	d.3+3=51	d.4+3=67

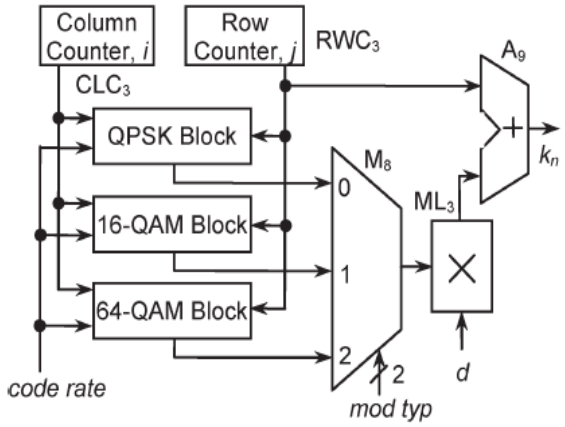

Fig 3: Complete deinterleaver address generator

VI Architecture of The Deinterleaver Address Generator

The complete deinterleaver address generator is shown in fig 1. Here QPSK block, 16 QAM block and 64 QAM block are presented. The common logic circuits such as multiplier, adder, row counter and column counter are shared while generating for any modulation technique. The design also shares the incrementer and decrementer required in 16 QAM ad 64 QAM blocks.

VII VITERBI TECHNIQUE

The viterbi algorithm is the maximum likelihood decoding procedure for Convolutional codes. The viterbi algorithm is used to find the sequence of hidden state as viterbi path. The algorithm can be applied to a host of problems encountered in the design of communication system. The operation of viterbi algorithm is through trellis diagram. By using trellis diagram the viterbi path determine the shortest path. The viterbi decoder begins after a certain number of encoded symbols have been received. A viterbi decoder uses the viterbi algorithm for decoding a bitstream. The viterbi decoding algorithm provides both maximum likelihood and maximum posterior algorithm. The Convolutional code is used to encode the bitstream. The major blocks of viterbi decoder are branch metric unit, path metric unit and trace back unit. There are hard decision and soft decision in viterbi decoder. A hard decision viterbi decoder receives a single bitstream on its input. A soft decision viterbi decoder receives a bitstream containing information about the reliability of each received signal. The viterbi decoding reduces the bit error rate.

VIII SIMULATION RESULT

The proposed hardware of the address generator is implemented using HDL VHDL using the Xilinx ISE. Simulation result is obtained for viterbi encoding/decoding and interleaver/deinterleaver using Modelsim 6.2c.

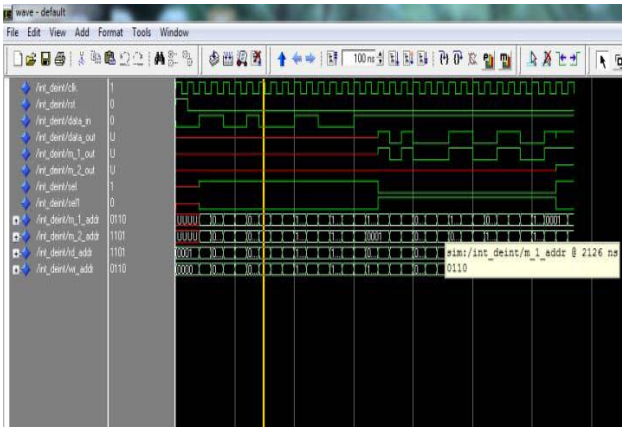

Fig 4: Simulation of Interleaver/deinterleaver

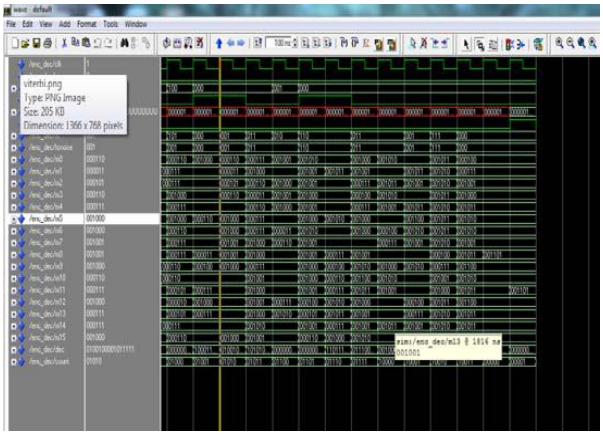

Fig 5: Viterbi technique

IX CONCLUSION

This paper has proposed an address generation for WiMAX deinterleaver. The WiMAX channel deinterleaver support all possible code rates. The proposed algorithm is converted into an optimized digital hardware circuit. The hardware is implemented on the Xilinx FPGA using VHDL.Compare to Reed Solomon technique, the viterbi technique reduces the error rate and time consumption.

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